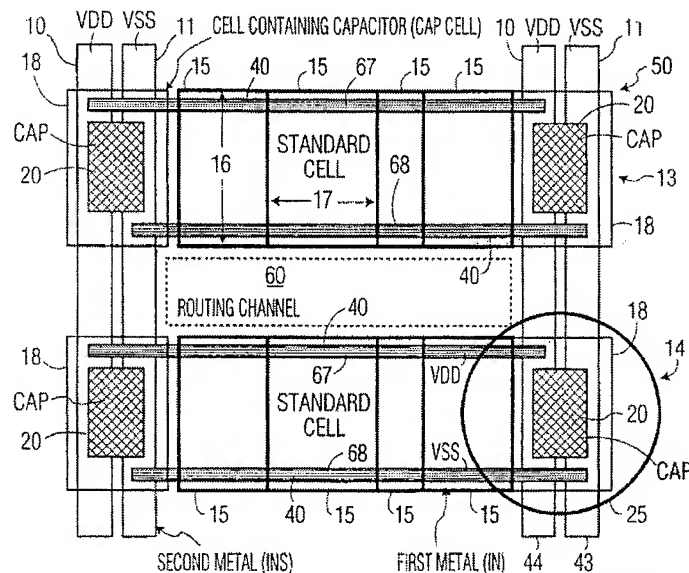


REMARKS

The non-final Office Action dated January 13, 2009 indicated the following new grounds of rejection: claims 1-8 and 10-20 stand rejected under 35 U.S.C. § 102(b) over Grzyb (U.S. Patent No. 5,656,834); and claims 1-20 stand rejected under 35 U.S.C. § 102(e) over Nassif (U.S. Patent Pub. 2004/0073881). Applicant traverses all rejections, and further does not acquiesce to any averments made in the Office Action, unless Applicant expressly indicates otherwise.

The § 102(b) rejection of claims 1-8 and 10-20 over the '834 reference is improper because the cited portions of the '834 reference do not appear to disclose any power pad or ground pad as claimed (or otherwise), and the Office Action has provided no explanation as to how any distance between such pads is maintained equal for different circuit elements. Referring to FIG. 1 upon which all rejections rely (copied below for convenience), the Office Action's assertions appear to confuse the shown distance between "power busses/rails" (VDD and VSS) with the claimed total combined distance between power and ground pads. As such pads are not shown in FIG. 1 and as the Office Action has provided no explanation as to how the respective VDD and VSS lines are connected, the Office Action's assertion that any circuit distance to power and ground pads is somehow equal is wholly unsupported.



Referring to FIG. 3 (copied below), it further appears that the distance between power and ground pads in the '834 reference would likely vary depending upon the cell location, and that the combined distances would not be equal as claimed. For instance, referring to the left-most portion of respective VDD and VSS lines, the total length of the circuit to cells in each of the vertical columns as represented in FIG. 3 would increase for those cells that are further away from the respective pads. While it is unclear as to where any pads are located, the respective distances to different circuit elements clearly varies.

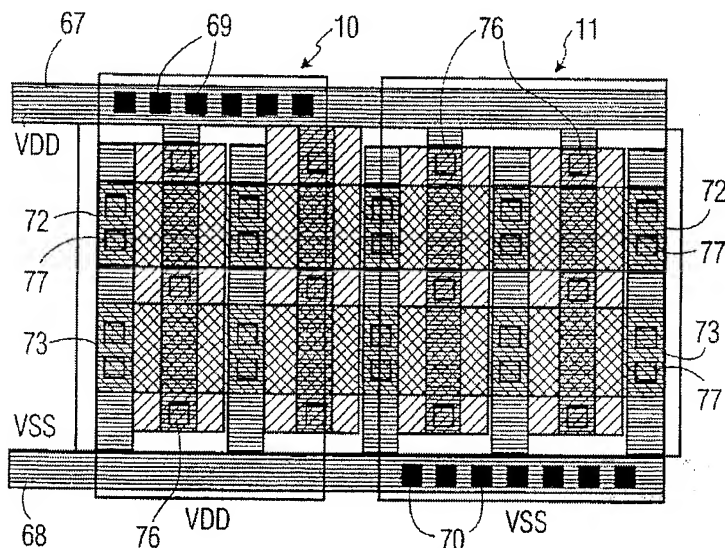


FIG. 3

In view of the above, Applicant believes that the Office Action has not established that the '834 reference discloses limitations directed to an equal combined circuit distance between power and ground pads for each circuit element. Accordingly, the Office Action has failed to establish correspondence under § 102(b) and the rejection should be removed.

Applicant further traverses the § 102(b) rejections of claims 11-12 because the rejections rely upon various assertions of allegedly inherent disclosure in the cited reference without providing any evidence in support thereof. To establish inherency, the extrinsic evidence “must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by

persons of ordinary skill.” *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (emphasis added). “Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *Id.* at 1269 (quoting *In re Oelrich*, 666 F.2d 578, 581 (C.C.P.A. 1981). In this instance, the Examiner’s assertion that the voltage drop in all of the circuit elements in the ‘834 reference would somehow be the same simply because each row has a symmetrical arrangement is contrary to the reference itself and well-understood circuit operation. As consistent with the above, it appears that the voltage drop (and other characteristics) would change depending upon the power/ground pad location, relative to FIG. 3 and/or as shown in FIG. 1. Applicant submits that the Office Action has therefore failed to establish that the limitations in claims 11-12 are inherently (necessarily) present in the cited reference.

The § 102(e) rejection of claims 1-20 over the ‘3881 reference is also improper because the cited circuit structure in FIG. 4, upon which all rejections rely, does not disclose any power or ground pads and further does not disclose that any distance to such power and ground pads would be equal for the circuit elements shown in FIG. 4. The Office Action appears to have again confused an equal distance between rails or busses with the claimed power network and its equal distance between power and ground pads that supply an entire integrated circuit chip. Reviewing FIG. 4 (copied below for convenience), no power or ground pads are shown, and the corresponding discussion does not reference any such pads or any distance thereto, as relevant to independent claims 1 and 14. Moreover, the respective rows appear to be arranged in a manner that would result in differing lengths between circuit elements from row to row as the distance increases for the particular row in question.

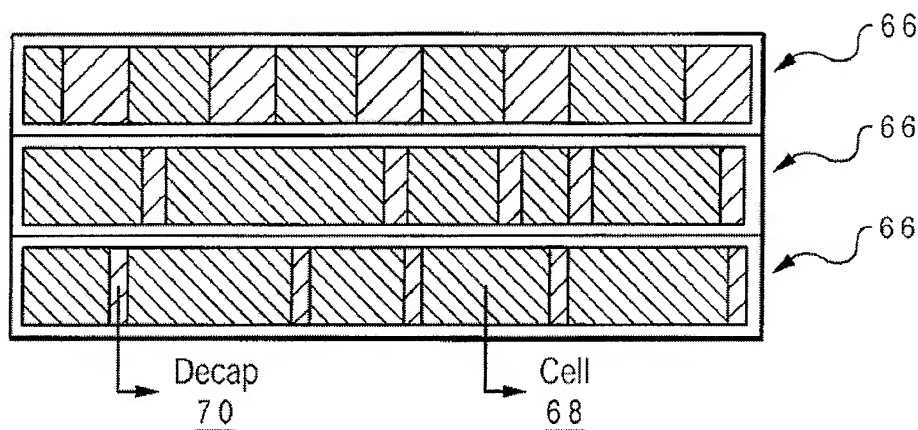


Fig. 4

Specifically regarding the rejection of claims 2-3, the Office Action's assertion that FIG. 4 somehow discloses power and ground pads on diagonally opposite corners of the IC is untenable, as no ground pads whatsoever are shown in FIG. 4. The Office Action similarly fails to show correspondence to limitations in various other dependent claims. Accordingly, the Office Action has failed to show correspondence between the '3881 reference and all claim limitations, in failing to show or explain any power and ground pads, and in failing to explain how such pads would be connected to various circuit elements.

The Office Action has also impermissibly rejected claims 14-20 over the '3881 reference without providing any explanation as to the rejections, by asserting that the claims "recite similar subject matter" to claims 1-13, yet failing address various limitations that are specific to claims 14-20. For example, no correspondence has been shown to limitations directed to decoupling cells maintaining any combined distances (*e.g.*, as in claims 15 and 16). Applicant has reviewed the '3881 reference and cannot ascertain any disclosure of limitations in all of claims 14-20.

In view of the above, the cited portions of the '3881 reference do not provide correspondence to the claimed invention, and further teach away from the same. Applicant therefore requests that the § 102(e) rejection be removed.

Applicant further traverses the § 102(e) rejection of claim 4, because the rejection relies upon allegedly inherent disclosure without providing any evidence in support

thereof. As discussed above, to establish inherency, the Office Action must provide extrinsic evidence that makes clear that the missing descriptive matter is necessarily present in the cited reference. In this instance, the Examiner's assertion that the claimed vertical and horizontal sections are inherent is similarly improper. As claimed, the combined distance between power and ground pads in all of the circuit elements is equal. As such, nothing in the '3881 reference would suggest that such an arrangement would necessarily be present. Furthermore, it appears that such an arrangement is not applicable, as the distance to different circuit elements in different rows would vary depending upon the placement of the pads. Accordingly, the § 102(e) rejection of claim 4 is also improper for these reasons.

Applicant also submits that the '3881 reference teaches away from the claimed approach to setting equal total distances, as the alleged "symmetrical" circuit elements in FIG. 4 are actually optimized to reduce noise by introducing *asymmetry*, to adjust space between circuit elements. As consistent with relevant case law (*see, e.g.,* M.P.E.P. § 2142, *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007)), "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." In this instance, the '3881 reference may "uniformly distribute the empty spaces in each row for an initial layout," but subsequently changes the spacing in response to "an adjoint sensitivity analysis." Referring to the discussion of FIG. 4 at paragraph 0032, "the present invention aims at changing the placement of cells 68 within row-oriented RLM structures such as those shown in FIG. 4 to allow decoupling capacitors 70 to be inserted" based on several variables, including those based upon differing power expenditures by each circuit element. Such changes may also be made to vary from what is initially set for "maintaining wire length" as described in paragraph 0034. Accordingly, the respective distances and decoupling capacitors in the '3881 reference are actually set to vary the combined distance for respective circuit elements in order to obtain noise optimization, which directly teaches away from the claimed invention.

Applicant has amended claim 4 to recite alternate language, in specifically reciting that different circuit elements are respectively connected between different interleaving bus sections, yet exhibit equal power bus to ground bus connectivity.

Support for these limitations may be found, for example, in FIG. 3 and described in connection therewith (*e.g.*, a circuit element at shown position x, y having equal power/ground pad distance, relative to a circuit element near reference number 63). As discussed above, none of the cited references disclose an integrated circuit with each given circuit element having an equal power to ground pad distance. Applicant thus submits that the cited references accordingly do not disclose such circuits in different rows. Applicant also notes that the orientation of horizontal/vertical lines is exemplary, such that the claim limitations are applicable to these and other orientations as consistent with the discussion in the specification regarding the same.

Applicant believes that each of the rejections and objections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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